

# **Analogue Devices and Techniques**

## **Amplifier Design**

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**February 8, 2000**

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## **ABSTRACT**

This report contains the design of an operational amplifier to meet certain specifications.

It includes all manual calculations which led to the design and simulation results to prove the design.

# **INTRODUCTION**

Since the advent of semi-conductors, the world of electronics has greatly advanced. Circuits are becoming smaller, using less power and hence lasting longer, when powered from batteries.

Amplifiers have existed since valve technology, however, nowadays an amplifier can be manufactured onto a single piece of silicon.

Operation Amplifiers (Op-amps) are such devices. They generally have differential inputs and a single ended output with a gain-bandwidth product in the MHz range. Op-amps are constructed with three stages:

1. Differential input stage - high differential gain and common mode rejection
2. Gain stage - high gain
3. Output stage - to increase drive capability

The purpose of this assignment was to design an operational amplifier out of discrete devices.

## WHAT IS AN OPERATIONAL AMPLIFIER?

Operational amplifiers are often used in instrumentation applications, for example sound sensors, motion sensors, temperature sensors etc. The output of the transducers are normally very small, i.e. milli or micro volts.

The transducers are often in electrically noisy environments, like factories and power stations etc. In order to reduce the amount of noise that the wires between the transducer and the op-amp pick up, differential transmission techniques are used. This is normally a twisted pair of wires, with or without shielding. As the wires are twisted together, the average distance between either wire and a noise source is the same. Hence any noise induced in one wire will be induced in the other wire.

Differential amplifiers amplify the *difference* between the two inputs, hence if the transducer is producing a 1mV differential, but 1V of noise is present on *both* wires (in phase) then only the true signal will be amplified. This is known as Common Mode Rejection.

Due to the nature of their design, differential amplifiers generally have a gain of up to 1000. For very small signals, this may not be sufficient to be of use to instrumentation, hence, a second stage of amplification is required. This is normally a Darlington type configuration to give a second gain of up to 1000, with more stages added if required. However, the Darlington output is of a very high impedance and as such cannot drive any significant loads.

To increase the drive capability of the amplifier, an output stage is added. There are many different configurations of output stages, for example an emitter follower. The output stage usually has a gain of 1, however, it can drive much larger loads than any other stage.

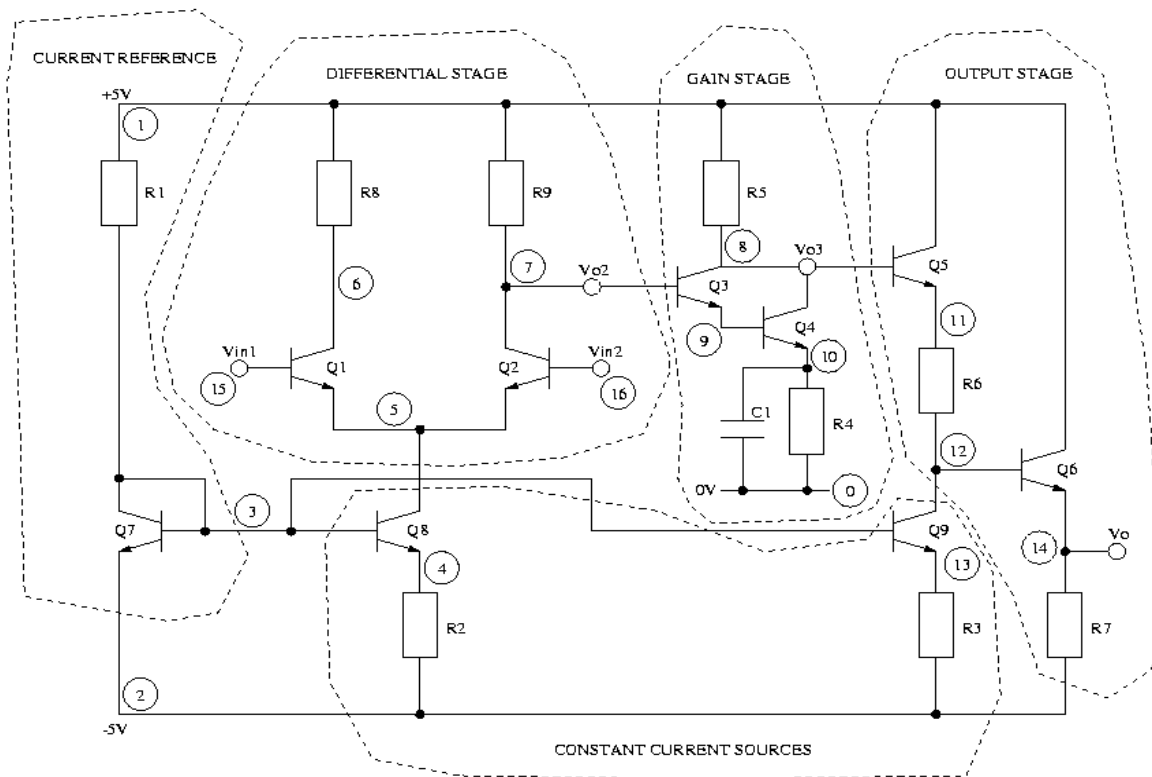
The stages are usually DC coupled together. This requires that the input of the second stage (for example) provide the bias current for the first stage and so on, so DC offset voltages and bias currents are critical to any design.

The feature of an op-amp that makes it special is the wide variety of ways that it can be used in a circuit. For example, it could be a simple amplifier, an inverting amplifier, a comparator, a differentiator, an integrator, etc.

# AMPLIFIER DESIGN

The op-amp designed for this experiment is shown in figure 1 below:

*Figure 1 - Amplifier circuit*



The numbers in circles are the node numbers used later in the report for the Spice netlist.

All transistors are BC337s which were chosen due to the student familiarity with them. They have the following basic parameters:

*Table 1 - BC337 transistor parameters*

Transistor	Type	Early Voltage, $V_A$	Forward Gain, $\beta$	Base-Emitter Voltage, $V_{BE}$
BC337	nnp	56.7 V	347	0.785 V

The op-amp was designed in 4 stages, firstly the current reference, then differential stage, gain stage and output stage.

## Current Reference

This section involves R1 and Q7.

The current  $I_{REF}$  required through the resistor was chosen as 1mA. Hence the value of resistor required is given by:

$$\begin{aligned} R_1 &= \frac{V_{SUP} - V_{BE7}}{I_{REF}} \\ &= \frac{10 - 0.785}{0.001} \\ &= 9215 \\ &\approx 9.2k\Omega \quad (\text{Ref.1 Equation 10.4}) \end{aligned}$$

## Differential Stage

This section involves R2, R8, R9, Q1, Q2, and Q8.

A quiescent current of 0.4mA flowing through R2 was decided upon. This required R2 to be the following value:

$$\begin{aligned} I_{R2} \times R_2 &= V_T \times \ln\left(\frac{I_{C3}}{I_{C8}}\right) \\ 0.4m \times R_2 &= 26m \times \ln\left(\frac{1m}{0.4m}\right) \\ R_2 &= \frac{26m \times \ln\left(\frac{1m}{0.4m}\right)}{0.4m} \\ \therefore R_2 &= 59.6\Omega \end{aligned}$$

(Ref.1 Equation 10.29)

With 0.4mA flowing through R2, 0.2mA must be flowing through each of the branches. If the two collector resistors, R8 and R9 are given values of 10k, then the DC output voltage of the differential stage,  $V_{o2}$  is given by:

$$\begin{aligned} V_{o2} &= V_{POS} - (I_{C2} \times R_9) \\ &= 5 - (0.2m \times 10k) \\ &= 3V \end{aligned}$$

This limits the common mode input voltage to:  $-4.3 \leq V_{CM} \leq 3$

## Gain Stage

Let  $I_{R4}$  be 0.4mA as well. Therefore, the value of  $R_4$  is as follows:

$$R_4 = \frac{V_{o2} - 2(V_{BE})}{0.4m}$$
$$\therefore R_4 = 4k\Omega$$

For the output of the gain stage to be half way between the supply and the input of the gain stage ( $V_{o2}$ ),  $V_{o3}$  must equal 4V, making  $R_5$  as follows:

$$R_5 = \frac{V_{POS} - V_{o2}}{I_{R5}}$$
$$= \frac{5 - 4}{0.4m}$$
$$\therefore R_5 = 2.5k\Omega$$

This will give a symmetrical voltage swing.

## Output Stage

Assuming that  $R_3 = R_2 = 59.6\Omega$ , then  $I_{R6} = I_Q = 0.4mA$ .

$Q_5$  and  $R_6$  allow a DC shift, therefore, to drop the voltage  $V_{B6}$  to 0.7V,  $R_6$  is:

$$V_{B6} = V_{o3} - V_{BE} - I_{R6} \times R_6$$
$$\therefore R_6 = \frac{V_{o3} - V_{BE} - V_{B6}}{I_{R6}}$$
$$= \frac{4 - 0.7 - 0.7}{0.4m}$$
$$\therefore R_6 = 6.5k\Omega$$

This will produce 0V output when 0V differential input is applied.

Finally, assume the current through  $R_7$  to be 2mA, then  $R_7$  is:

$$R_7 = \frac{V_o - V_{NEG}}{I_{R7}}$$
$$= \frac{0 - (-5)}{2m}$$
$$\therefore R_7 = 2.5k\Omega$$

## AC Analysis

The gain of the op-amp can be expressed as:

$$A_d = A_{d1} \times A_2 \times A_3$$
$$= \left( \frac{V_{o2}}{V_{in1} - V_{in2}} \right) \times \left( \frac{V_{o3}}{V_{o2}} \right) \times \left( \frac{V_o}{V_{o3}} \right)$$

(Ref.1 Example 11.16)

Where  $A_{d1}$  is the gain of the differential stage,  $A_2$  the gain stage and  $A_3$  the output stage.

$$A_{d1} = \left( \frac{V_{o2}}{V_{in1} - V_{in2}} \right)$$
$$= \frac{g_m}{2} (R_9 // R_{i2})$$

(Ref.1 Example 11.16)

Where  $R_{i2}$  is the input resistance of the Darlington pair:

$$R_{i2} = r_{\pi3} + (1 + \beta)r_{\pi4} \quad (\text{Ref.1 Example 11.16})$$

Where:

$$r_{\pi4} = \frac{\beta \times V_T}{I_{R4}}$$
$$= \frac{347 \times 26m}{0.4m}$$
$$\therefore r_{\pi4} = 22.555k\Omega$$

$$r_{\pi3} = \frac{\beta^2 \times V_T}{I_{R4}}$$
$$= \frac{(347)^2 \times 26m}{0.4m}$$
$$\therefore r_{\pi3} = 7.827M\Omega \quad (\text{Ref.1 Example 11.16})$$

Therefore:

$$R_{i2} = 7.827M + (1 + 347) \times 22.555k$$
$$\therefore R_{i2} = 15.676M\Omega \quad (\text{Ref.1 Example 11.16})$$

Since  $R_9 \gg R_{i2}$ , we can ignore  $R_{i2}$  as it is so high it will not affect the differential stage.

$$\begin{aligned}
 g_m &= \frac{I_Q}{2 \times V_T} \\
 &= \frac{0.4m}{2 \times 26m} \\
 \therefore g_m &= 7.69mS \quad (\text{Ref.1 Example 11.16})
 \end{aligned}$$

Therefore:

$$\begin{aligned}
 A_{d1} &= \frac{g_m}{2} (R_9 // R_{i2}) \\
 &= \frac{7.69m}{2} \times 10k \\
 \therefore A_{d1} &= 38.45 \quad (\text{Ref.1 Example 11.16})
 \end{aligned}$$

For the Darlington section (gain stage):

$$\begin{aligned}
 A_2 &= - \left( \frac{I_{R4}}{2 \times V_T} \right) (R_5 // R_{i3}) \\
 & \quad (\text{Ref.1 Example 11.16})
 \end{aligned}$$

Where  $R_{i3}$  is the input resistance of the output stage:

$$\begin{aligned}
 R_{i3} &= r_{\pi5} + (1 + \beta) \left[ R_6 + r_{\pi6} + (1 + \beta) R_7 \right] \\
 & \quad (\text{Ref.1 Example 11.16})
 \end{aligned}$$

Where:

$$\begin{aligned}
 r_{\pi5} &= \frac{\beta \times V_T}{I_{R6}} \\
 &= \frac{347 \times 26m}{0.4m} \\
 \therefore r_{\pi5} &= 22.555k\Omega
 \end{aligned}$$

$$\begin{aligned}
 r_{\pi6} &= \frac{\beta \times V_T}{I_{R7}} \\
 &= \frac{347 \times 26m}{2m} \\
 \therefore r_{\pi6} &= 4511\Omega \quad (\text{Ref.1 Example 11.16})
 \end{aligned}$$

Therefore:

$$R_{i3} = 22.555k + 348 \left[ 6.5k + 4511 + 348(2.5k) \right]$$

$$\therefore R_{i3} = 306.61M\Omega \quad (\text{Ref.1 Example 11.16})$$

Since  $R_5 \gg R_{i3}$ , we can ignore  $R_{i3}$  as it is so high it will not affect the gain stage.

Therefore:

$$A_2 = - \left( \frac{I_{R4}}{2 \times V_T} \right) (R_5 // R_{i3})$$

$$= - \left( \frac{0.4m}{2 \times 26m} \right) \times 2.5k$$

$$\therefore A_2 = 19.23 \quad (\text{Ref.1 Example 11.16})$$

The output stage is an emitter follower, hence  $V_o = V_{o3}$ , therefore gain  $A_3 = 1$ . The overall gain the then:

$$A_d = A_{d1} \times A_2 \times A_3$$

$$= 38.45 \times 19.23 \times 1$$

$$\therefore A_d = 739.39$$

$$= 57.4dB$$

The Common Mode Rejection Ratio of the circuit is given by:

$$CMRR = \left| \frac{A_{d1}}{A_{CM}} \right| = \frac{1}{2} \left[ 1 + \frac{(1 + \beta) \times I_Q \times R_o}{V_T \times \beta} \right]$$

$$(\text{Ref.1 Equation 11.35})$$

Where  $R_o$  is the output resistance of the Widlar current source:

$$R_o = r_{o8} + R_2$$

$$= \frac{V_A}{I_{C8}} + R_2$$

$$= \frac{56.7}{0.4m} + 59.6$$

$$\therefore R_o = 141.81k\Omega$$

Therefore:

$$CMRR = \frac{1}{2} \left[ 1 + \frac{(1+347) \times 0.4m \times 141.81k}{26m \times 347} \right]$$

$$\begin{aligned} \therefore CMRR &= 1094.5 \\ &= 60.8dB \end{aligned}$$

# ANALYSIS OF CIRCUIT

The circuit was analyzed using AIM Spice on a PC. See appendix A for the Spice netlist of the circuit.

Initially, the capacitor C1, was omitted from the design as no hint of capacitor value was given in the design book. Doing this, the circuit did not perform as expected in the gain stage. Applying an AC waveform of 1mV to the  $V_{in1}$  input while holding  $V_{in2}$  at 0V, the following was obtained:

*Table 2 - Gains of stages*

Measured Point	AC Voltage	Gain of Stage
Vo2	41mV	41
Vo3	25mV	<b>0.6</b>
Vo	24mV	1 (approx)

Capacitor C1 was added, starting at a nominal 50nF. It was noted that the gain increased at the higher frequencies to the calculated gain. By increasing the capacitor value, the lower cut-off frequency tended to 0. At this point, a capacitor of 47000uF was in the circuit, resulting in a flat response from 0 up to 10kHz.

The DC offset voltages were then examined and found to be approximately the calculated results. Any differences were due to the base-emitter voltage not being exactly calculated, i.e. 0.7V was taken during some calculations. Also, the reference current,  $I_{REF}$  is not exactly 1mA due to the rounding error in selecting the resistor value. The offset voltage of the output  $V_o$  was -0.15V. This was adjusted by varying the value of R6 from 6.5k to 6.1k. Shown below in figure 2 are all DC voltages in the circuit:

*Figure 2 - DC offset voltages*

Variables in circuit	Values
v(1)	5 Volt
v(2)	-5 Volt
v(15)	0 Volt
v(16)	0 Volt
v(13)	-4.97691 Volt
v(12)	0.695027 Volt
v(3)	-4.32077 Volt
v(8)	3.80559 Volt
v(11)	3.1472 Volt
v(14)	0.0017381 Volt
v(7)	3.11677 Volt
v(9)	2.54453 Volt
v(10)	1.88264 Volt
v(4)	-4.97767 Volt
v(5)	-0.641195 Volt
v(6)	3.12407 Volt
v(q7.collector)	-4.32175 Volt
v(q7.emitter)	-4.99982 Volt
v(q2.collector)	3.11658 Volt

v(q2.collector)	3.11658 Volt
v(q2.emitter)	-0.64116 Volt
v(q1.collector)	3.12388 Volt
v(q1.emitter)	-0.64116 Volt
v(q8.collector)	-0.64158 Volt
v(q8.emitter)	-4.9776 Volt
v(q4.collector)	3.80512 Volt
v(q4.emitter)	1.88273 Volt
v(q3.collector)	3.80558 Volt
v(q3.emitter)	2.54453 Volt
v(q6.collector)	4.99802 Volt
v(q6.emitter)	0.00210223 Volt
v(q5.collector)	4.99961 Volt
v(q5.emitter)	3.14727 Volt
v(q9.collector)	0.694647 Volt
v(q9.emitter)	-4.97683 Volt
i(vin2)	-4.84101E-006 Amp
i(vin1)	-4.84101E-006 Amp
i(vneg)	0.00377879 Amp
i(vpos)	-0.00423977 Amp

As can be seen, the new output offset voltage  $V_o$  which is  $V(14)$ , i.e. node 14, is 1.7mV. The other voltages of importance to note are  $V(7)$  which is  $V_{o2}$  in calculations and  $V(8)$  which is  $V_{o3}$ . These are approximately 3V and 4V respectively, as calculated.

The input offset voltage is thus:

$$V_{Ioff} = \frac{V_{Ooff}}{A_v} = \frac{1.7m}{1120} = 1.5\mu V$$

The input and output AC analysis waveform from each stage are shown below in figures 3 to 5:

Figure 3 - Differential stage

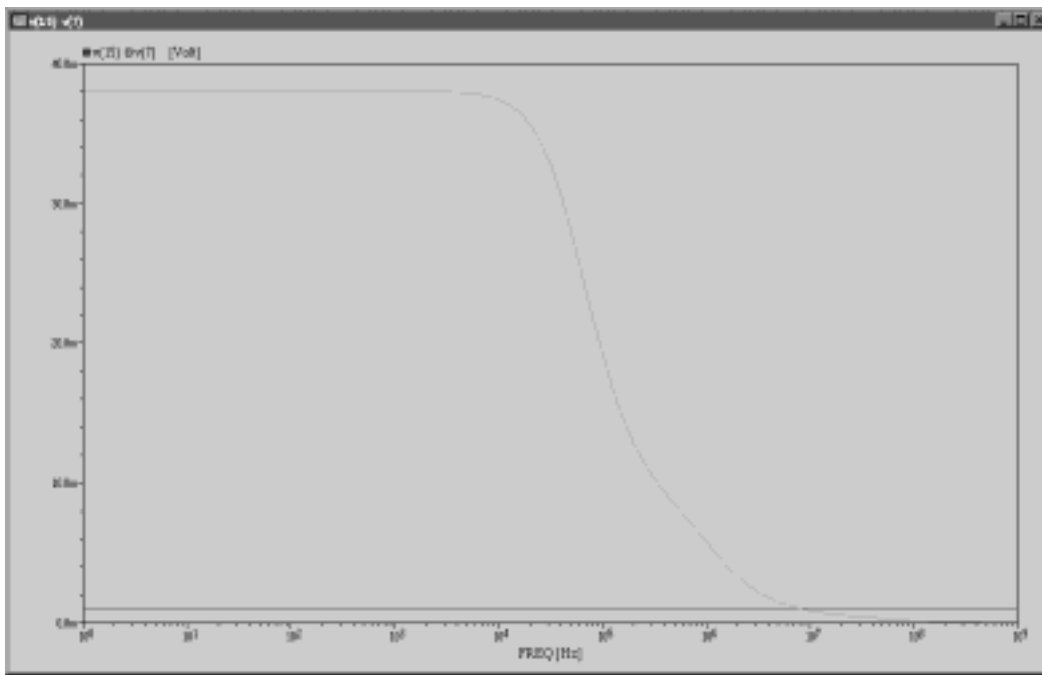


Figure 4 - Gain stage

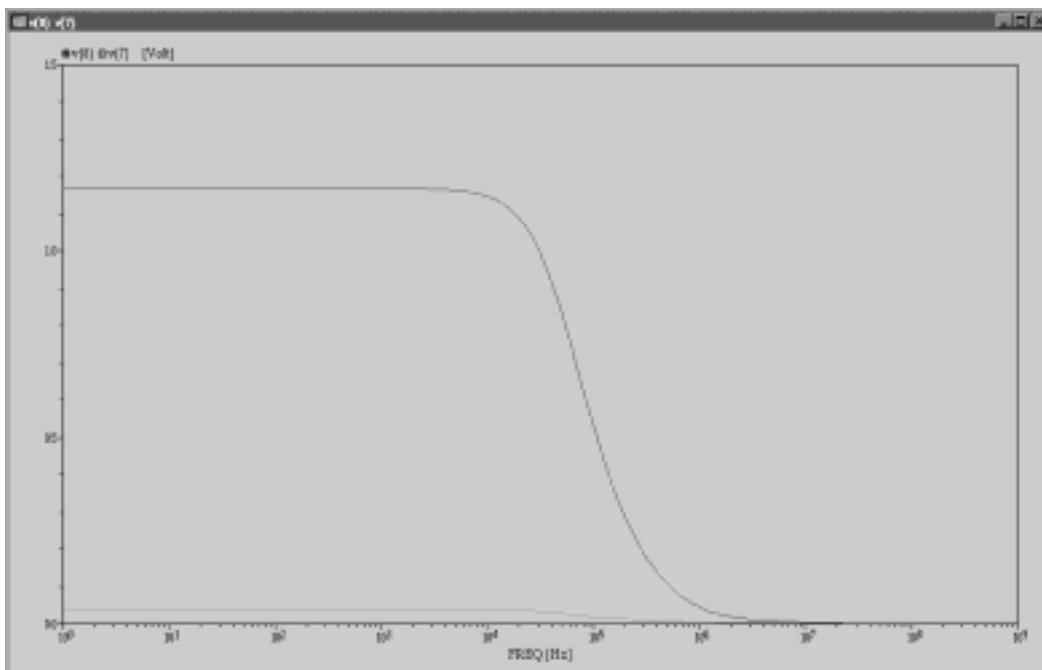
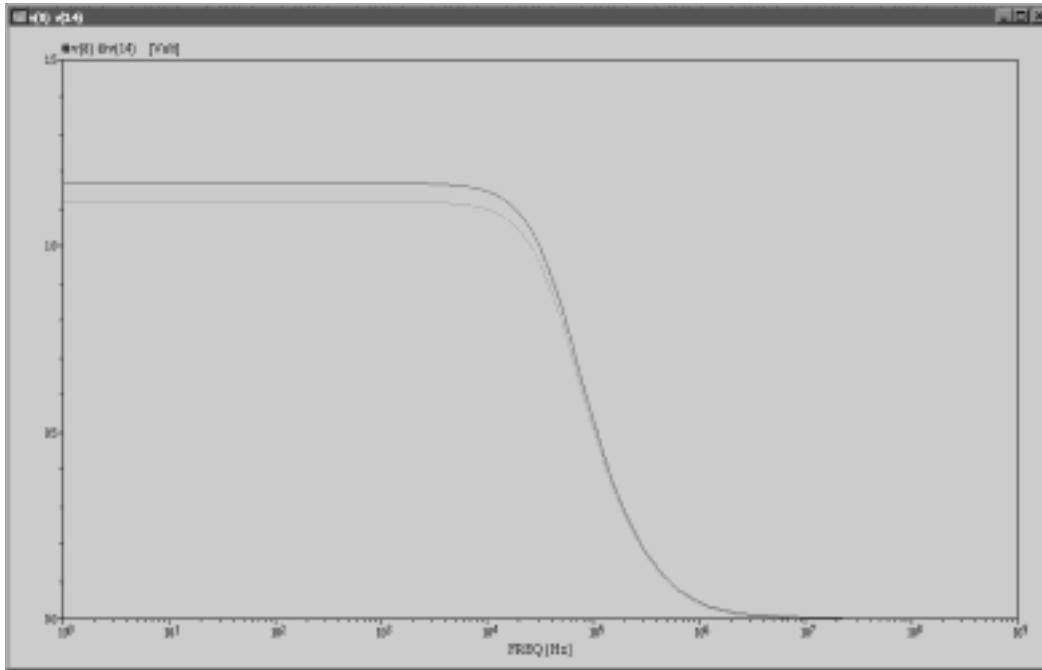


Figure 5 - Output stage



The gains of the various stages are shown below in table 3:

Table 3 - Final gains of stages

Measured Point	AC Voltage	Gain of Stage
Vo2	38mV	38
Vo3	1.17V	30
Vo	1.12V	1 (approx)

The overall gain of the amplifier is:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{1.12}{1m} = 1120 = 61 \text{ dB}$$

This is far better than the expected gain of the amplifier which was 739. This is due to the rounding errors performed during the calculations compared to the accuracy of the model used in the spice deck as a full set of spice parameters were used.

The gain-bandwidth product of the amplifier is:

$$V_{oMAX} = 1.12V$$

$$\frac{1}{2} \text{power point} = \frac{V_{oMAX}}{\sqrt{2}}$$

$$= \frac{1.12}{\sqrt{2}}$$

$$= 0.79V$$

*Frequency at  $\frac{1}{2}$  power  $\approx 50\text{kHz}$*

$$\begin{aligned}\therefore \text{GBP} &= \text{Gain} \times \text{Bandwidth} \\ &= 1120 \times 50\text{k} \\ &= 56\text{MHz}\end{aligned}$$

# CONCLUSION

The circuit, when simulated, performed much better than expected due to calculation assumptions and approximations.

It met most of the requirements placed upon it. Below is a table of comparison between requirements and achieved results:

*Table 3 - Requirements comparison*

Parameter	Required	Achieved
Voltage Gain	>60dB	61dB
Gain Bandwidth Product	1MHz	56MHz
Common Mode Rejection Ratio	1%	60.8dB
Power Supply	+/- 5V	+/- 5V
Output Current	>100uA	2mA
Output Swing	+/- 1V	+/- 1.12V
Input Offset Voltage	< +/- 25uV	1.5uV
Power Dissipation	< 1mW	>1mW
Slew Rate	> 2V/us	<2V/us

The student has learned how important bias currents and DC offsets are in designing a DC coupled amplifier, which without careful calculation, could prevent the circuit from functioning.

During this investigation, the student discovered many configurations of amplifier ranging from the relatively simple design in this report to very complex designs involving active loads and combinations of bi-polar and CMOS technology.

There is still a lot of material on analogue electronics that the student can learn about. This investigation into amplifiers has started the student on his quest into the analogue world.

## **REFERENCES**

1. Electronic Circuit Analysis and Design, Donald A Neamen, WCB/McGraw-Hill, 1996, ISBN 0071143564.
2. AIM Spice - <http://www.eece.napier.ac.uk/~analogue/files/aimspice.exe>

# APPENDIX A - Spice Netlist

Operational Amplifier

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\* Power Supply

VPOS 1 0 DC 5V  
VNEG 2 0 DC -5V

\* Input Signal

VIn1 15 0 AC 1m  
VIn2 16 0 DC 0

\* Output Stage

R3 13 2 59.6  
Q9 12 3 13 BJTNP  
Q5 1 8 11 BJTNP  
R6 11 12 6.1k  
Q6 1 12 14 BJTNP  
R7 14 2 2.5k

\* Gain Stage

Q3 8 7 9 BJTNP  
Q4 8 9 10 BJTNP  
R5 1 8 2.5k  
R4 10 0 4k  
C1 10 0 47000u

\* Differential Stage

R2 4 2 56.9  
Q8 5 3 4 BJTNP  
R8 1 6 10k  
R9 1 7 10k  
Q1 6 15 5 BJTNP  
Q2 7 16 5 BJTNP

\* 1mA Reference Current Source

R1 1 3 9.2K  
Q7 3 3 2 BJTNP

\* Model for the BC337 transistor

.MODEL BJTNP NPN(IS=4.35e-17 NF=0.853 NR=0.853 RE=0.182 RC=1 VAF=56.7 VAR=28.3  
+ ISE=287f ISC=287f NE=1.5 NC=1.5 BF=347 BR=5 IKF=0.198 IKF=0.198  
+ CJC=12.3p CJE=33p VJC=0.273 VJE 0.785 TF=758p TR=98.5n KF=0 AF=1)

# APPENDIX B - FINAL SCHEMATIC

